

Fig. 1A  
(Prior Art)

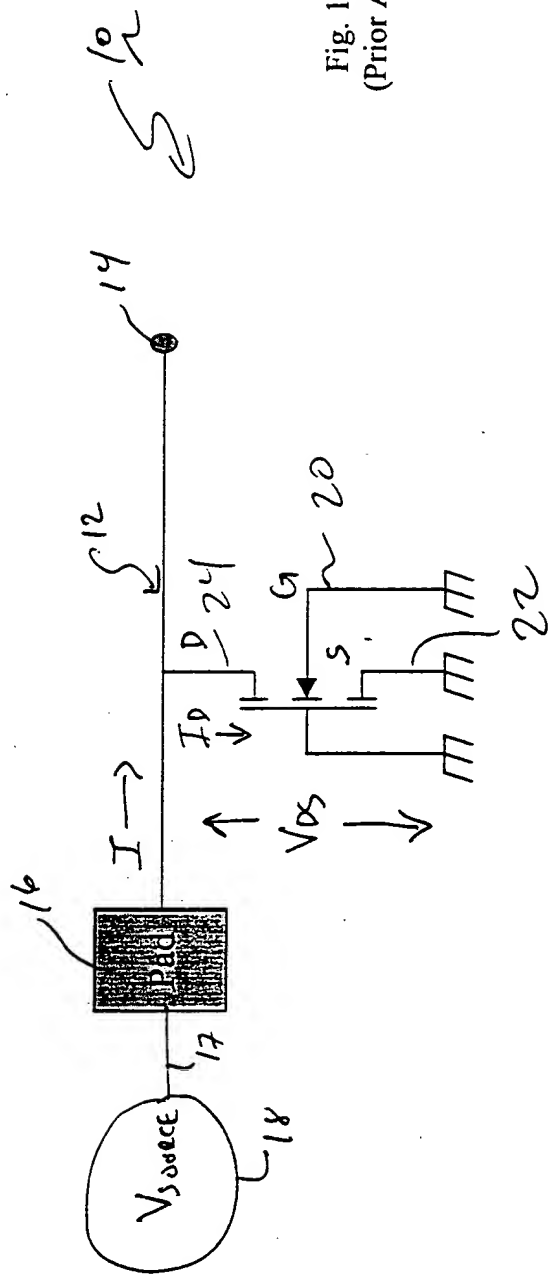
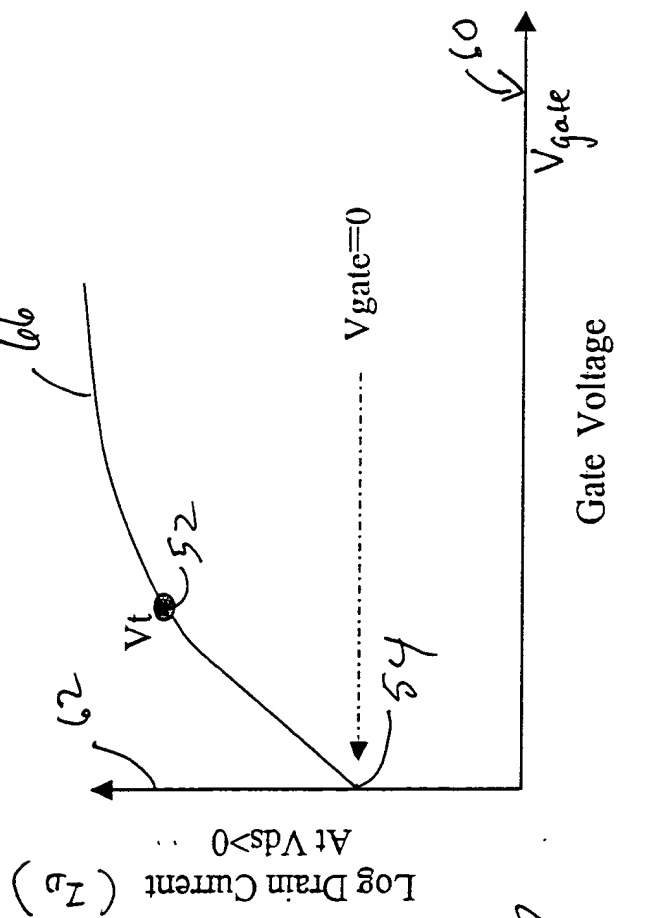


Fig. 1B  
(Prior Art)



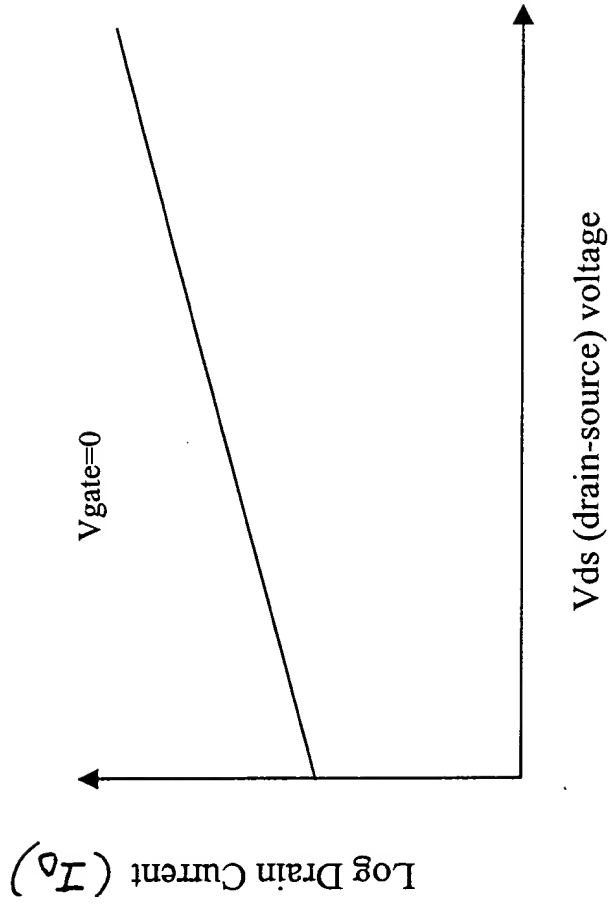


Fig. 1C  
(Prior Art)



FIG. 3 is a schematic diagram of a circuit for protecting low voltage devices from electrostatic discharge (ESD) damage. The circuit includes a series of input protection devices (80a, 80b, ..., 80n) connected to a common input line. Each input protection device (80a, 80b, ..., 80n) consists of a diode (12a, 12b, ..., 12n) connected to ground and a transistor (m) connected to a voltage source (Vsource\_a, Vsource\_b, ..., Vsource\_n). The input protection devices are connected to a series of low voltage devices (152) to be protected. The low voltage devices are represented by a series of rectangular blocks connected in a chain. The input protection devices are connected to the low voltage devices through a series of connection points. The input protection devices are connected to the low voltage devices through a series of connection points. The input protection devices are connected to the low voltage devices through a series of connection points.

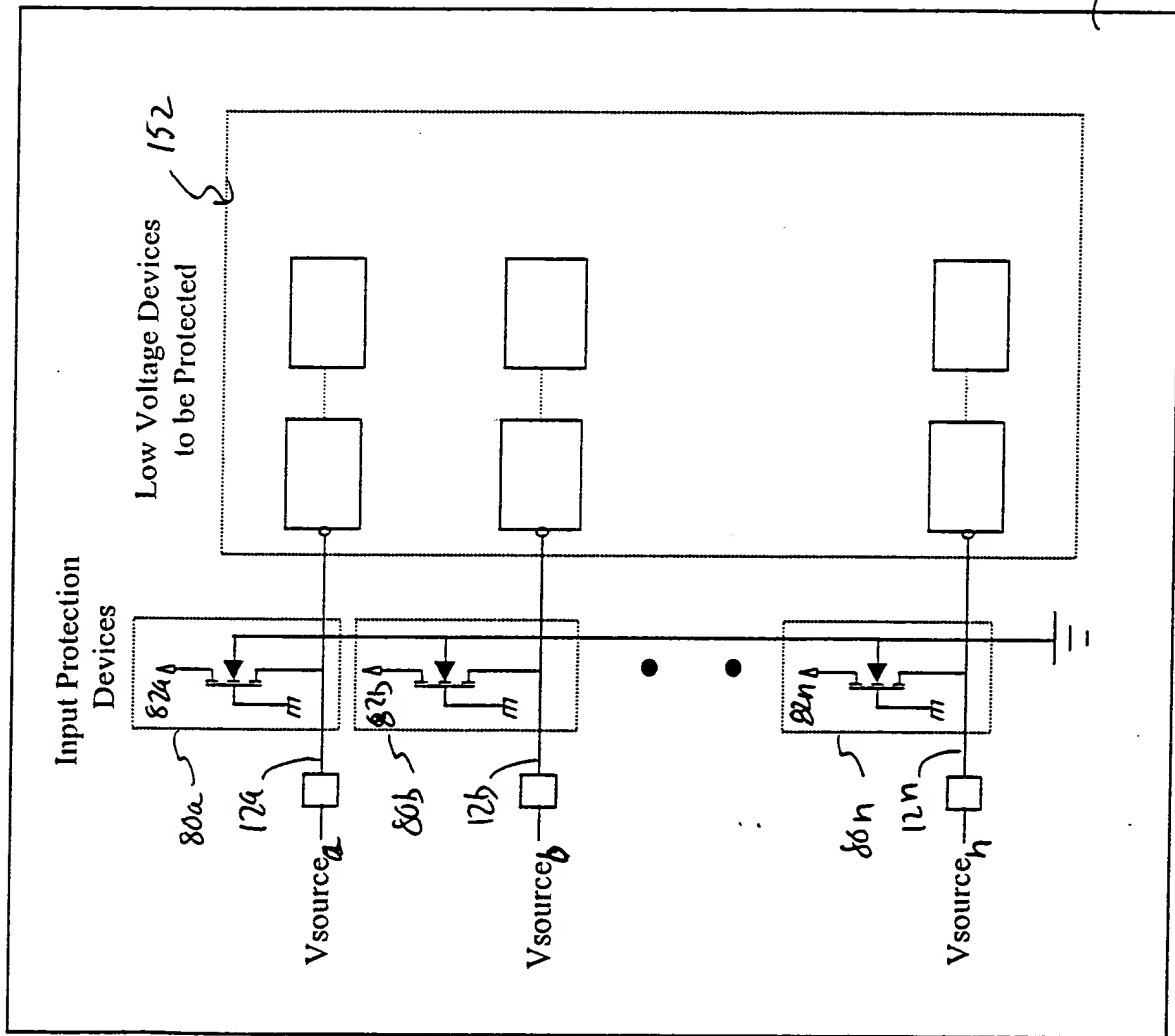


Fig. 3

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